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MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL (AMD)
P.O. BOX 398
AUSTIN, TX 78767-0398

EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 09/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,551	WISOR, MICHAEL T.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/5/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is in responsive to communication filed on 5 August 2004 and 4 November 2005.

2. Notice of change of address placed in File Wrapper.

3. Claims 1 – 37 are presented for the examination.

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 5 August 2004 was filed before the mailing date of the first office action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claims 1 – 36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. The claim language of an independent claim 1 is totally confusing because the relationship among, "a first vendor generating one or more files corresponding to an integrated circuit, the integrated circuit having one or more registers, wherein a content of the one or more files is structured for at least one of:" "incorporation into boot code sequence", and "access by the boot code sequence during execution" is insufficiently defined or incomplete for omitting essential structural cooperative relationships of

elements, such omission amounting to a gap between the necessary structural connections or showing insufficiency or missing essential elements or steps to define the relationship among them. See MPEP § 2172.01.

7. The claim language of an independent claim 21 is totally confusing because the relationship among generated, "generate one or more files corresponding to an integrated circuit, the integrated circuit having one or more registers, wherein a content of the one or more files is structured for at least one of:" "incorporation into boot code sequence", and "access by the boot code sequence during execution" is insufficiently defined or incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections or showing insufficiency or missing essential elements or steps to define the relationship among them. See MPEP § 2172.01.

8. The claim language of an independent claim 35 is totally confusing because the relationship among, "receiving, from a first vendor, one or more files corresponding to an integrated circuit designed by the first vendor, the integrated circuit having one or more registers, wherein a content of the one or more files is structured for at least one of," "incorporation into boot code sequence", and "access by the boot code sequence during execution" is insufficiently defined or incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections or showing insufficiency or missing essential elements or steps to define the relationship among them. See MPEP § 2172.01.

9. The claim language of an independent claim 36 is totally confusing because the relationship among, "one or more files corresponding to an integrated circuit, the integrated circuit having one or more registers, wherein a content of the one or more files is structured for at least one of:" "incorporation into boot code sequence", and "access by the boot code sequence during execution" is insufficiently defined or is incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections or showing insufficiency or missing essential elements or steps to define the relationship among them. See MPEP § 2172.01.

10. Claim 25 recites the limitation "the vendor is one of a plurality of vendors----" in lines 1-2 on page 31. There is insufficient antecedent basis for this limitation in the claim 21.

11. Claims 2 – 20 and 22 – 34 are dependent on independent claims 1 and 21 respectively, and therefore are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

12. Claims 1 – 36 are rejected under 35 U.S.C. 101 in light of 35 U.S.C. 112, second paragraph rejection, raises a question as to whether the claim is directed merely to an abstract idea that is not tied to a technological art, environment or machine which would

result in a practical application producing a concrete, useful, and tangible results to form the basis of statutory subject matter under 35 U.S.C. 101.

13. Claims 21 – 34, and 36, are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Specifically, the claims 21 – 34, and 36, are directed to "computer accessible medium" which is broad enough to read on as "media accessible via transmission media" or "signals" as per definition in specification in lines 8 – 15 on page 27. A claimed signal is clearly not a "process" under 35 U.S.C. 101 because it is not a series of steps. A claimed signal has no physical structure, does not itself perform any useful, concrete and tangible result and, does not fit within the definition of a machine. A claimed signal is not matter, but a form of energy, and therefore is not a composition of matter. A signal, a form of energy, does not fall within one of the four statutory classes of 35 U.S.C. 101. This can be overcome by amending in claims 21 – 36 as "computer accessible storage media".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 1 – 37, are rejected under 35 U.S.C. 102(b) as being clearly anticipated by applicant admitted prior art [hereinafter as AAPA].

15. As to claim 1, AAPA discloses a method comprising a first vendor [vendor] generating [developed] one or more files [BIOS/boot code] corresponding to an

integrated circuit [specifications, lines 5 – 7 on page 2], the integrated circuit having one or more [various] registers [specification, lines 1 – 2, and 13 – 15, on page 2], wherein a content of the one or more files [BIOS/boot code] is structured [in specification, lines 14 – 24] for at least one of: (i) incorporation into a boot code sequence [specifications, lines 10- 23 on page 3]; or (ii) access [fetch] by the boot code sequence during execution [code can be fetched by processor fetched and executed]; and wherein the boot code sequence is configured to initialize [by writing initial values into] the one or more [various] registers responsive to the content during execution [of POST][specifications, pages 1 – 7, and steps: 34, 52, and 58 in fig. 2, 3, 4 respectively].

16. As to claim 21, AAPA discloses a method to initialize registers in various integrated circuits in a computer system during a booting computer including a computer accessible medium [non-volatile memory/ROM/Flash] comprising a first one or more instructions [BIOS/boot instructions] which, when executed [during boot] generate one or more files [configuration files] corresponding to an integrated circuit [lines 16 – 20 on page 6], the integrated circuit having one or more [various] registers [specification, lines 1 – 2, and 13 – 15, on page 2], wherein a content of the one or more files [BIOS/boot code] is structured [in specification, lines 14 – 24] for at least one of: (i) incorporation into a boot code sequence [specifications, lines 10- 23 on page 3]; or (ii) access [fetch] by the boot code sequence during execution [code can be fetched by processor and executed]; and wherein the boot code sequence is configured to initialize [by writing initial values into] the one or more [various] registers responsive to the

content during execution [of POST][specifications, pages 1 – 7, and steps: 34, 52, and 58 in fig. 2, 3, and 4 respectively].

17. As to claim 35, AAPA discloses receiving, from [provided by] a first vendor, one or more files [BIOS/boot code] corresponding to an integrated circuit designed by the first vendor [specifications, lines 5 – 17 on page 2], the integrated circuit having one or more [various] registers [specification, lines 1 – 2, and 13 – 15, on page 2], wherein a content of the one or more files [BIOS/boot code] is structured [in specification, lines 14 – 24] for at least one of: (i) incorporation into a boot code sequence [specifications, lines 10- 23 on page 3]; or (ii) access [fetch] by the boot code sequence during execution [code can be fetched by processor fetched and executed]; and wherein the boot code sequence is configured to initialize [by writing initial values into] the one or more [various] registers responsive to the content during execution [of POST][specifications, pages 1 – 7, and steps: 34, 52, and 58 in fig. 2, 3, and 4 respectively]; and incorporating the content of the one or more files into the boot code sequence [specifications, lines 10- 23 on page 3].

18. As to claim 36, AAPA discloses a computer accessible medium [non-volatile memory/ROM/Flash] comprising one or more files [configuration files] corresponding to an integrated circuit [lines 16 – 20 on page 6], the integrated circuit having one or more [various] registers [specification, lines 1 – 2, and 13 – 15, on page 2], wherein a content of the one or more files [BIOS/boot code] is structured [in specification, lines 14 – 24] for at least one of: (i) incorporation into a boot code sequence [specifications, lines 10- 23 on page 3]; or (ii) access [fetch] by the boot code sequence during execution [code can

be fetched by processor and executed in POST][specifications, pages 1 – 7, and steps: 34, 52, and 58 in fig. 2, 3, and 4 respectively].

19. As to claim 37, AAPA discloses a system [computer system] comprising:

a. one or more integrated circuits [processors, chipset components such as the north bridge and south bridge components etc. in specification, lines 27 –28 on page 1], at least one of which comprises a processor; and one or more nonvolatile memories [ROM/Flash] storing: (i) a boot code sequence executable by the processor [specification, lines16 – 18 on page 1] and (ii) one or more files [configuration files] corresponding to at least a first integrated circuit [lines 16 – 20 on page 6] of the one or more integrated circuits [processors, chipset components such as the north bridge and south bridge components etc. in specification, lines 27 –28 on page 1], the first integrated circuit having one or more [various] registers [specification, lines 1 – 2, and 13 – 15, on page 2], wherein a content of the one or more files [BIOS/boot code] is structured [in sequence] for access by the boot code sequence during execution [POST] [code can be fetched by processor and executed in POST][specifications, pages 1 – 7, and steps: 34, 52, and 58 in fig. 2, 3, and 4 respectively]; wherein the boot code sequence is configured to initialize [by writing initial values into] the one or more [various] registers responsive to the content during execution [of POST][specifications, pages 1 – 7, and steps: 34, 52, and 58 in fig. 2, 3, and 4 respectively].

20. As to claim, 2, AAPA teaches to perform a change to the one or more files without requiring a recompile of the boot code sequence [specifications, lines 21 – 23 on page 3].

21. As to claim 3, AAPA teaches the first vendor [integrated circuit vendor] transmitting [providing] the one or more files [documentation of the registers in integrated circuit, and values which registers are to be initialized by the BIOS code] [lines 13 – 17 on page 2] to second vendor BIOS vendor] [specifications lines 5 – 17 on page 2].

22. As to claim 4, AAPA teaches the second vendor [BIOS vendor] is one of a plurality of vendors [Phoenix, Award, and American Megatrends, Inc. (AMI)] that develop the boot code sequence [specifications17 – 18 on page 2], and wherein the generating the one or more files comprises providing a plurality of sections in the one or more files, each of the plurality of sections corresponding to a different one of the plurality of vendors [specifications lines 5 – 25].

23. As to claim 5, AAPA teaches the first vendor [integrated circuit vendor] transmitting [providing] the one or more files [documentation of the registers in integrated circuit, and values which registers are to be initialized by the BIOS code] [lines 13 – 17] to a manufacturer of a system that includes the integrated circuit and the boot code sequence [specifications lines 5 – 17 on page 2].

24. As to claim 6, AAPA teaches to store the one or more files [boot code sequence] in a nonvolatile memory [ROM/flash] in the system [specifications, lines 16 – 18 on page 1].

25. As to claim 7, AAPA discloses a computer system boot-up, which inherently teaches accessing the one or more files during execution of the boot code sequence in the system.

26. As to claim 8, AAPA teaches the boot code sequence is divided into a plurality of phases [an early phase [fig. 2], a middle phase [fig. 3] subsequent to the early phase, and a late phase [fig. 4] subsequent to the middle phase], and wherein the one or more files are also divided according to the plurality of phases, and wherein generating the one or more files comprises including a first register of the one or more registers in a first phase of the plurality of phases in which the first register is to be initialized [specifications, pages 3 – 5, figs. 1 – 4].

27. As to claim 9, AAPA teaches the boot code sequence is divided into a plurality of phases including an early phase [fig. 2], a middle phase [fig. 3] subsequent to the early phase, and a late phase [fig. 4] subsequent to the middle phase [specifications, pages 3 – 5, figs. 1 – 4].

28. As to claim 10, AAPA teaches one or more files comprise at least one table of register identifiers [each entry in table defines register] [lines 5 – 7 on page 6] and corresponding initialization values [values to be programmed into register] for the one or more registers [specification, lines 5 – 7].

29. As to claim 11, AAPA teaches one or more files [boot code] comprise code [BIOS sequence] which, when executed, initializes at least one register of the one or more registers [specification, 5 – 10 on page 4, lines 10 – 13 on page 6].

30. As to claim 12, AAPA teaches one or more files comprises code [boot code sequence routine] which, when executed, initializes at least one register of the one or more [various] registers [specification, 5 – 10 on page 4, lines 10 – 13 on page 6].

31. As to claim 13, AAPA teaches incorporating [inserting] the code [custom code] from the one or more files into the boot code sequence during a compile of the boot code sequence [specification lines 14 – 23 on page 3].

32. As to claim 14, AAPA teaches a database [a data table] corresponding to the integrated circuit defines the one or more registers and initialization values [values to be programmed] for the one or more registers, and wherein generating one or more files comprises parsing the database [routine that reads each and every entry in table] to extract indications of the one or more registers, and the initialization values [specification lines 5 – 14].

33. As to claim 15, AAPA teaches the database [data table] further defines temporal ordering requirements [POST code] for at least some of the one or more registers, and wherein the first instructions [Start BIOS] further comprise a third one or more instructions [Early POST, Middle POST, Late POST] which, when executed, order the indications of the one or more registers [Early POST register, Middle POST register, Late POST register] and the initialization values [register initialization] according to the temporal ordering requirements [POST code][fig. 1 - 4].

34. As to claim 16, AAPA teaches a first temporal ordering requirement [Early POST] corresponding to a first register [Early POST register] of the one or more registers identifies a first phase [Early POST phase] of a plurality [Early POST, Middle POST, Late POST] of phases of the boot code sequence in which the first register [Early POST register] is to be initialized [specifications pages 2 – 6, step 34, fig. 2].

35. As to claim 17, AAPA teaches a first temporal ordering requirement [Early POST] corresponding to a first register [Early POST register] of the one or more registers [Early POST register, Middle POST register, Late POST register] identifies [as defined in data table] a second register of the one or more registers and an order [boot sequence routine] of initializing the first register and the second register [specifications lines 5 – 14 on page 6].

36. As to claim 18, AAPA teaches the integrated circuit [processor] includes a plurality of blocks [routines], each block having a subset of the one or more [various] registers, and a first temporal ordering requirement [Early POST] corresponding to a first register [Early POST register] of the one or more registers [Early POST register, Middle POST register, Late POST register] identifies [as defined in data table] a second register of the one or more registers and an order [boot sequence routine] of initializing the first register and the second register [specifications lines 5 – 14 on page 6].

37. As to claim 19, AAPA teaches the database [a data table] further includes at least one initialization indication of whether or not initialization is required [mask defining which bits of the register to update], the parsing not extracting a corresponding indication of a first register in response to the initialization indication indicating that initialization of the first register is not required [specification, lines 7 – 10 on page 6].

38. As to claim 20, AAPA teaches the first vendor [integrated circuit vendor] designs [provides documentation of the registers in the integrated circuit and values to which the registers are to be initialized by BIOS code] the integrated circuit [specification lines 13 – 15].

39. As to claim 22, AAPA teaches the computer accessible medium [non-volatile memory/ROM/Flash] including a second one or more instructions which, when executed, transmit [providing] the one or more files [documentation of the registers in integrated circuit, and values which registers are to be initialized by the BIOS code] [lines 13 – 17 on page 2] to second vendor BIOS vendor] [specifications lines 5 – 17 on page 2] to at least one of: (i) a vendor [Phoenix, Award, and American Megatrends, Inc. (AMI)] that develops the boot code sequence [specifications17 – 18 on page 2]; or (ii) a manufacturer of a system [OEMs] that includes the integrated circuit and the boot code sequence [specifications lines 5 – 25].

40. As to claim 23, AAPA teaches the boot code sequence is divided into a plurality of phases [an early phase [fig. 2], a middle phase [fig. 3] subsequent to the early phase, and a late phase [fig. 4] subsequent to the middle phase], and wherein the one or more files are also divided according to the plurality of phases, and wherein generating the one or more files comprises including a first register of the one or more registers in a first phase of the plurality of phases in which the first register is to be initialized [specifications, pages 3 – 5, figs. 1 – 4].

41. As to claim 24, AAPA teaches the boot code sequence is divided into a plurality of phases including an early phase [fig. 2], a middle phase [fig. 3] subsequent to the early phase, and a late phase [fig. 4] subsequent to the middle phase [specifications, pages 3 – 5, figs. 1 – 4].

42. As to claim 25, AAPA teaches a vendor [BIOS vendor] is one of a plurality of vendors [BIOS vendors, Phoenix, Award, AMI, etc.] that develop the boot code

sequence [BIOS code], and wherein first instructions comprise one or more instructions [inherent to BIOS code] which, when executed, provide a plurality of sections [registers] in the one or more files [values], each of the plurality of sections [registers] corresponding to a different one of the plurality of vendors [registers to be initialized with values provided by vendors][specifications, lines 5 – 25 on page 2].

43. As to claim 26, AAPA teaches one or more files comprise at least one table of register identifiers [each entry in table defines register] [lines 5 – 7 on page 6] and corresponding initialization values [values to be programmed into register] for the one or more registers [specification, lines 5 – 7].

44. As to claim 27, AAPA teaches one or more files [boot code] comprise code [BIOS sequence] which, when executed, initializes at least one register of the one or more registers [specification, 5 – 10 on page 4, lines 10 – 13 on page 6].

45. As to claim 28, AAPA teaches one or more files comprises code [boot code sequence routine] which, when executed, initializes at least one register of the one or more [various] registers [specification, 5 – 10 on page 4, lines 10 – 13 on page 6].

46. As to claim 29, AAPA teaches a database [a data table] corresponding to the integrated circuit defines the one or more registers and initialization values [values to be programmed] for the one or more registers, and wherein the first instructions comprises a third one or more instructions which, when executed, parsing the database [routine that reads each and every entry in table] to extract indications of the one or more registers, and the initialization values [specification lines 5 – 14 on page 6].

47. As to claim 30, AAPA teaches the computer accessible medium [non-volatile memory/ROM/Flash] wherein the database [data table] further defines temporal ordering requirements [POST code] for at least some of the one or more registers, and wherein the first instructions [Start BIOS] further comprise a third one or more instructions [Early POST, Middle POST, Late POST] which, when executed, order the indications of the one or more registers [Early POST register, Middle POST register, Late POST register] and the initialization values [register initialization] according to the temporal ordering requirements [POST code][fig. 1 - 4].

48. As to claim 31, AAPA teaches the computer accessible medium [non-volatile memory/ROM/Flash] wherein a first temporal ordering requirement [Early POST] corresponding to a first register [Early POST register] of the one or more registers identifies a first phase [Early POST phase] of a plurality [Early POST, Middle POST, Late POST] of phases of the boot code sequence in which the first register [Early POST register] is to be initialized [specifications pages 2 – 6, step 34, fig. 2].

49. As to claim 32, AAPA teaches the computer accessible medium [non-volatile memory/ROM/Flash] wherein a first temporal ordering requirement [Early POST] corresponding to a first register [Early POST register] of the one or more registers [Early POST register, Middle POST register, Late POST register] identifies [as defined in data table] a second register of the one or more registers and an order [boot sequence routine] of initializing the first register and the second register [specifications lines 5 – 14 on page 6].

50. As to claim 33, AAPA teaches the computer accessible medium [non-volatile memory/ROM/Flash] wherein the integrated circuit [processor] includes a plurality of blocks [routines], each block having a subset of the one or more [various] registers, and a first temporal ordering requirement [Early POST] corresponding to a first register [Early POST register] of the one or more registers [Early POST register, Middle POST register, Late POST register] identifies [as defined in data table] a second register of the one or more registers and an order [boot sequence routine] of initializing the first register and the second register [specifications lines 5 – 14 on page 6].

51. As to claim 34, AAPA teaches the database [a data table] further includes at least one initialization indication of whether or not initialization is required [mask defining which bits of the register to update], and wherein the third one or more instructions, when executed, do not extract a corresponding indication of a first register in response to the initialization indication indicating that initialization of the first register is not required [specification, lines 7 – 10 on page 6].

52. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

53. Claim 36 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Yu et al. [hereinafter as Yu], US Patent 6,865,670 B2.

54. As to claim 36, Yu discloses a computer accessible medium [120 hard disk] comprising one or more files [system enabler files] corresponding [specific] to an integrated circuit [hardware, which inherently includes integrated circuit, processor 110] [col. 4, lines 8 – 12], the integrated circuit [110, processor], having one or more registers [registers are inherent to the processor], wherein a content [patches, code, data, resources needed to utilizes specific new hardware] of the one or more files [system enabler files] [col. 6, lines 5 – 10] is structured for at least one of: (i) incorporation into [by moving out of read only memory (ROM) into files] a boot code sequence [boot or start-up routine/procedure][col. 3, lines 60 – 64, col. 10, lines 33 – 40]; or (ii) access [booting continue by locating] by the boot code sequence [boot or start-up routine/procedure] during execution [boot][col. 5, lines 8 – 24, col. 6, lines 54 – 59, fig. 1].

55. As to claim 37, Yu discloses a system [140 computer system] comprising: one or more integrated circuits [110 CPU, 116 ROM, 114 RAM, fig. 1], at least one of which comprises a processor [110, CPU]; and one or more nonvolatile memories [116 ROM, 120 hard disk] storing: (i) a boot code sequence [boot or start-up routine/procedure] executable by the processor [110] and (ii) one or more files [system enabler files] corresponding [specific] to a first integrated circuit [hardware, which inherently includes integrated circuit, processor 110] [col. 4, lines 8 – 12] of the one or more integrated circuits [110 CPU, 116 ROM, 114 RAM, fig. 1], the firs integrated circuit [110,

processor], having one or more registers [registers are inherent to the processor], wherein a content [patches, code, data, resources needed to utilizes specific new hardware] of the one or more files [system enabler files] [col. 6, lines 5 – 10] is structured for access [booting continue by locating] by the boot code sequence [boot or start-up routine/procedure] during execution [boot][col. 5, lines 8 – 24, col. 6, lines 54 – 59, fig. 1]; wherein the boot code sequence [boot or start-up routine/procedure] is configured to initialize the one or more registers responsive to the content [col. 9, lines 60 – 67, col. 10, lines 8 – 67, col. 11, lines 1 – 6, col.13, lines 30 – 41, col. 14, lines 1 – 6].

56. **Examiner's note**: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

57. **Prior Art not relied upon**: Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Nitin C. Patel 9/5/06
Nitin C. Patel
Patent Examiner
Technology Centre 2100